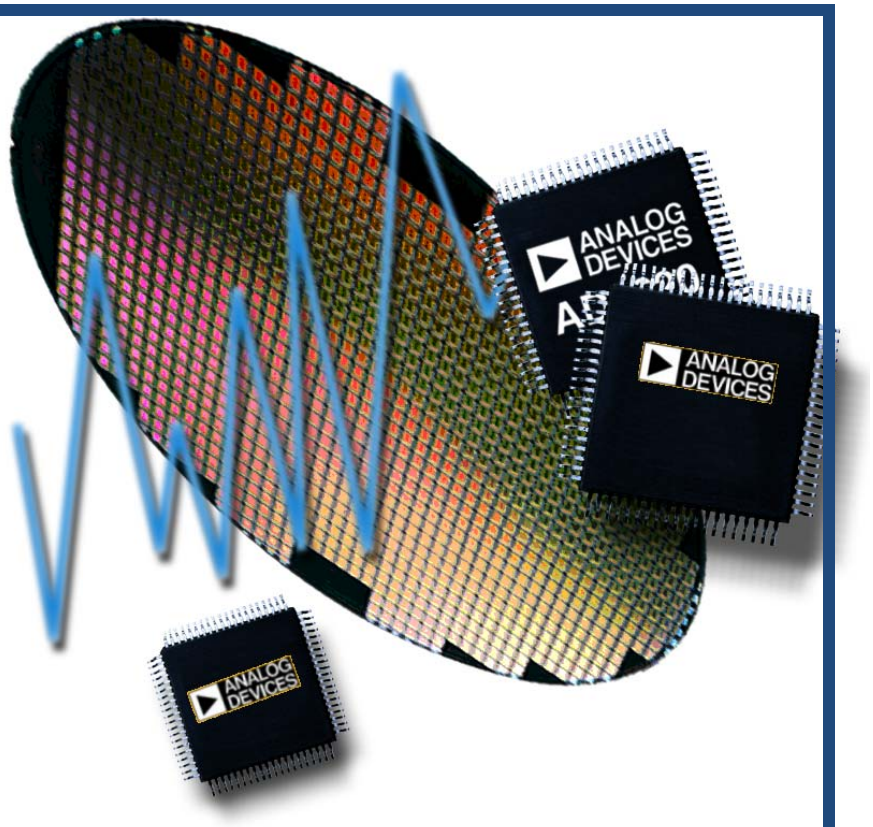

Reliability Report

Report Title: ADuM540x Die Revision E Qualification

Report Number: 9023

Revision: A

Date: 10 November 2010

Summary

This report documents the successful completion of the reliability qualification requirements for release of the ADuM540x revision E family of products in a 16-SOIC_W package.

The ADuM540x is a 4-die architecture product: IC1 and IC2 are fabricated on 0.6um CMOS at ADI-Limerick, ADuM1400TC is fabricated on 0.35um at TSMC (then goes to ChipBond for 1M post processing at ChipBond) and ADuM5400TC is fabricated on the 3M post processing at ChipBond. The revision E consisted in metal mask changes on IC2 to fix start up issues.

The ADuM540x device is a quad-channel digital isolator with *iso*Power®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides up to 500 mW of regulated, isolated power with 5.0 V input and 5.0 V output voltages. This architecture eliminates the need for a separate, isolated dc-to-dc converter in low power, isolated designs. The *i*Coupler chip scale transformer technology is used to isolate the logic signals and the magnetic components of the dc-to-dc converter. The result is a small form factor, total isolation solution.

Table 1: ADuM540x Product Characteristics

Die/Fab

Die ID	ADuM5400IC1 rev B	ADuM5400IC2 rev E	ADuM5400TC	ADuM1400TC rev A
Die Size (mm)	1.43 x 2.90	1.40 x 3.17	1.50 x 3.20	1.12 x 2.76
Wafer Fabrication Site	ADI Limerick		ChipBond	TSMC 3C
Wafer Fabrication Process	0.6um HV CMOS	0.6um DPTM CMOS	3M Isolator Process	0.35um 1M
Transistor Count	1 thousand	1 thousand	0	0
Passivation Layer	undoped-oxide/SiN		None	undoped-oxide/OxyNitride
Bond Pad Metal Composition	AlCu			
Die Overcoat	NA		Polyimide	Polyimide (1M ChipBond)

Package/Assembly

Available Package	16-SOIC_W
Body Size (mm)	10.30 x 7.50 x 2.40
Assembly Location	Carsem-S
Molding Compound	Sumitomo 6600H
Wire Type	Gold Tanaka M3
Wire Diameter (mils)	1.30
Die Overcoat	NA
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Lead Finish	Matte Sn
Moisture Sensitivity Level	3
Maximum Peak Reflow Temperature (°C)	260

Description / Results of Tests Performed

Tables 2 and 3 provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: SOIC_W at Carsem-S Package Qualification Test Results

Test Name	Spec	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
Autoclave (AC)[1]	JESD22-A102	121°C 100%RH 2atm 96 hours	ADuM1410	Carsem-S 16-SOIC_W	Q6806.1	77	0
					Q6806.5	77	0
			ADuM5230		Q6502.1	77	0
					Q6502.4	77	0
					Q6502.7	77	0
			ADuM5400		Q6503.1	77	0
			ADuM6132		Q6986.1	77	0
					Q6986.2	77	0
					Q6986.3	77	0
			ADuM5400		Q7492.5	77	0
					Q7492.6	77	0
					Q7492.7	77	0
Autoclave (AC)[2]		121°C 100%RH 2atm 200 hours	ADuM5401		Q8550.42	77	0
					Q8550.43	77	0
		121°C 100%RH 2atm 96 hours	ADuM5400		Q8550.41	77	0
Biased HAST (HAST)[1]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	ADuM1410		Q6805.10	77	0
					Q6805.6	77	0
					Q6806.10	77	0
					Q6806.6	77	0
			ADuM1402		Q7616.1	77	0
					Q7616.10	77	0
					Q7971.4	77	0
			ADuM5400		Q7492.10	77	0
					Q7492.8	77	0
					Q7492.9	77	0
Biased HAST (HAST)[2]					Q8550.25	77	0
					Q8550.26	77	0
					Q8550.27	77	0
Biased HAST (HAST)[1]			ADuM7410		Q7233.7	77	0
					Q7233.9	77	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C 1,000 hours	ADuM5400		Q8550.10	77	0
Solder Heat Resistance (SHR)[2]	ADI-0049	See Footer	ADuM6200		Q8369.1	30	0
Solder Heat Resistance (SHR)[1]			ADuM5400		Q7492.12	11	0
					Q7492.13	11	0
					Q7492.14	11	0

Test Name	Spec	Conditions	Device	Package	Lot #	Sample Size	Qty. Failures
Solder Heat Resistance (SHR)[2]	ADI-0049	See Footer	ADuM5400	Carsem-S 16-SOIC_W	Q8550.34	11	0
					Q8550.35	11	0
					Q8550.36	11	0
Temperature Cycling (TC)[1]	JESD22-A104	-65°C / +150°C 500 cycles	ADuM1410		Q6805.12	77	0
					Q6805.8	77	0
			ADuM5230		Q6502.2	77	0
					Q6502.5	77	0
					Q6502.8	77	0
			ADuM5400		Q6503.4	77	0
			ADuM6132		Q6986.10	77	0
					Q6986.11	77	0
					Q6986.9	77	0
			ADuM5400		Q7492.15	77	0
					Q7492.16	77	0
					Q7492.17	77	0
Temperature Cycling (TC)[2]					Q8550.31	77	0
					Q8550.32	77	0
					Q8550.33	77	0

1) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

2) These Samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 192 hrs @ 30ºC, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.

Table 3: 0.6µm CMOS at ADI Limerick Fab Qualification Test Results

Test Name	Spec	Conditions	Device	Fab Process	Lot #	Sample Size	Qty. Failures
Early Life Failure Rate (ELFR)[1]	MIL-STD-883, Method 1015	125°C 48 hours	ADuM5400W	ADI Limerick 0.6µm CMOS	Q7771.18	84	0
					Q7771.27	77	0
					Q7771.19	84	0
					Q7771.21	125	0
					Q7771.20	77	0
					Q7771.22	77	0
					Q7771.23	77	0
					Q7771.24	77	0
					Q7771.25	77	0
					Q7771.26	77	0
					Q7771.28	77	0
					Q7771.29	77	0
					Q7771.30	77	0
					Q7771.31	77	0
					Q7771.32	77	0
					Q7771.33	77	0
					Q7771.34	77	0
					Q7771.35	77	0
					Q7771.36	62	0
					Q7771.37	77	0
					Q7771.38	77	0
					Q7771.39	77	0
					Q7771.40	77	0
					Q7771.42	77	0
					Q7771.43	77	0
					Q7771.44	77	0
					Q7771.45	77	0
Biased HAST (HAST)[2,3]	JESD22-A110	130°C 85%RH 2atm, Biased 96 hours	ADuM5400		Q7492.9	77	0
					Q7492.10	77	0
Biased HAST (HAST)[4]					Q7492.8	77	0
					Q6503.47	77	0
					Q6503.48	77	0
Biased HAST (HAST)[4,3]					Q6503.50	77	0
					Q8550.25	77	0
					Q8550.26	77	0
					Q8550.27	77	0
Biased HAST (HAST)[4,5]			ADuM5400W		Q7771.1	77	0
					Q7771.2	77	0
					Q7771.3	77	0
High Temperature Operating Life (HTOL)[3]	JESD22-A108	125°C ‹ Tj ‹ 135°C, Biased 1,000 hours	ADUM5400		Q7671.23	45	0
					Q7671.22	45	0
					Q7671.24	45	0
High Temperature Operating Life (HTOL)					Q6503.33	77	0
					Q6503.34	77	0
					Q6503.35	77	0
High Temperature Operating Life (HTOL)[2]			ADuM5230		Q6502.14	77	0
					Q6502.15	77	0
					Q6502.16	77	0
High Temperature Operating Life (HTOL)[4,1]			ADuM5400W		Q7771.6	77	0
					Q7771.4	77	0
High Temperature Operating Life (HTOL)[4,3]		150°C ‹ Tj ‹ 175°C, Biased 500 hours	ADuM5400		Q8550.37	77	0
					Q8550.38	77	0
					Q8550.39	77	0

Test Name	Spec	Conditions	Device	Fab Process	Lot #	Sample Size	Qty. Failures
High Temperature Storage Life (HTSL)[3]	JESD22-A103	150°C 1,000 hours	ADUM5400	ADI Limerick 0.6µm CMOS	Q7671.231	45	0
					Q8550.10	77	0
High Temperature Storage Life (HTSL)[5]			ADuM5401W		Q7771.7	45	0
High Temperature Storage Life (HTSL)[3]			ADUM5230		Q6502.17	77	0
			ADUM5400		Q6503.13	77	0
					Q7492.11	77	0
					Q6503.39	77	0

1) Pre- and post-stress electrical test was performed at hot, ambient and cold temperatures.
2) These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 168 hrs @ 85ºC, 85%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.
3) Electrical test was performed at ambient temperatures.
4) These Samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125ºC, Soak: Unbiased Soak: 192 hrs @ 30ºC, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260ºC.
5) Pre- and post-stress electrical test was performed at ambient and hot temperatures.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

ESD Test Results

The results of Human Body Model (HBM), Machine Model (MM), and Field Induced Charge Device Model (FICDM) ESD testing are summarized in the ESD Results Table. ADI measures ESD results using stringent test procedures based on the specifications listed. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook (available via the 'Quality and Reliability' link at the Analog Devices' web site).

Table 5: ESD Test Results (ADuM5400)

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	16-SOIC_W	JESD22-C101	1Ω, Cpkg	±1500V	NA	C6
HBM		JESD22-A114	1.5kΩ, 100pF	±2000V	NA	2
MM		JESD22-A115	0Ω, 200pF	±200V	NA	M3

Latch-Up Test Results

Six samples of the ADuM5400 were Latch-up tested at T_A=25ºC per JEDEC Standard JESD78, Class I, Level A. All six devices passed.

Approvals

This report has been approved by electronic means (5.0).
Reliability Engineer: Arnaud Sow

Additional Information

Data sheets and other additional information are available on Analog Devices' web site.